What is claimed is:

1. A semiconductor integrated circuit, comprising:

a phase control circuit to which a first clock signal is inputted, and which shifts a phase of the first clock signal based on a phase control signal and outputs the resultant signal as a second clock signal;

a first flip-flop to which one of the first clock signal and the second clock signal is inputted as a first operation clock signal, and which operates in synchronization with an edge of the inputted first operation clock signal and outputs evaluation data;

a circuit under test to which the evaluation data is inputted, and which performs a predetermined process based on the evaluation data and outputs a result of the process as output data; and

a second flip-flop to which the other of the first clock signal and the second clock signal is inputted as a second operation clock signal and the output data is inputted, and which operates in synchronization with an edge of the inputted second operation clock signal and outputs the output data inputted from the circuit under test.

2. The semiconductor integrated circuit according to claim 1, wherein the phase control signal is inputted from outside of the semiconductor integrated circuit.

3. The semiconductor integrated circuit according to claim 2, wherein in a normal operation, the phase control signal such that the first clock signal and the second clock signal are synchronized is inputted.

4. The semiconductor integrated circuit according to claim 3, wherein in an operation test, the phase control signal such that a phase difference is formed between the first clock signal and the second clock signal is inputted.

5. A control method of a semiconductor integrated circuit, comprising:

controlling a phase control circuit based on a phase control signal to shift a phase of a first clock signal and outputting the resultant signal as a second clock signal;

inputting one of the first clock signal and the second clock signal as a first operation clock signal to a first flip-flop, operating the first flip-flop in synchronization with an edge of the inputted first operation clock signal, and outputting evaluation data;

inputting the evaluation data to a circuit under test, performing a predetermined process based on the evaluation data, and outputting a result of the process as output data; and

inputting the other of the first clock signal and the second clock signal as a second operation clock signal to a second flip-flop and inputting the output data, operating the second flip-flop in synchronization with an edge of the inputted second clock signal, and outputting the output data inputted from the circuit under test.

6. The control method of the semiconductor integrated circuit according to claim 5, further comprising inputting the phase control signal from outside of the semiconductor integrated circuit.

7. The control method of the semiconductor integrated circuit according to claim 6, wherein in a normal operation, the phase control signal such that the first clock signal and the second clock signal are synchronized is inputted.

8. The control method of the semiconductor integrated circuit according to claim 7, wherein in an operation test, the phase control signal such that a phase difference is formed between the first clock signal and the second clock signal is inputted.

9. A semiconductor integrated circuit, comprising:

a phase control circuit to which a first clock signal is inputted, and which shifts a phase of the first clock signal based on a phase control signal and outputs the resultant signal as a second clock signal;

a first selector to which the first clock signal and the second clock signal are inputted, and which outputs one of the first clock signal and the second clock signal as a first operation clock signal based on a first selector control signal;

a first flip-flop to which the first operation clock signal is inputted, and which operates in synchronization with an edge of the first operation clock signal and outputs evaluation data;

a circuit under test to which the evaluation data is inputted, and which performs a predetermined process based on the evaluation data and outputs a result of the process as output data;

a second selector to which the first clock signal and the second clock signal are inputted, and which outputs the other of the first clock signal and the second clock signal as a second operation clock signal based on a second selector control signal; and

a second flip-flop to which the second operation clock signal is inputted and the output data is inputted, and which operates in synchronization with an edge of the second operation clock signal and outputs the output data inputted from the circuit under test.

10. The semiconductor integrated circuit according to claim 9, wherein the phase control signal, the first selector control signal, and the second selector control signal are inputted from outside of the semiconductor integrated circuit.

11. The semiconductor integrated circuit according to claim 10, wherein in a normal operation, the phase control signal, the first selector control signal, and the second selector control signal such that the first clock signal and the second clock signal are synchronized are inputted.

12. The semiconductor integrated circuit according to claim 11, wherein in an operation test, the phase control signal, the first selector control signal, and the second selector control signal such that a phase difference is formed between the first clock signal and the second clock signal are inputted.

13. A control method of a semiconductor integrated circuit, comprising:

controlling a phase control circuit based on a phase control signal to shift a phase of a first clock signal and outputting the resultant signal as a second clock signal;

controlling a first selector based on a first selector control signal to output one of the first clock signal and the second clock signal as a first operation clock signal;

inputting the first operation clock signal to a first flip-flop, operating the first flip-flop in synchronization with an edge of the first operation clock signal, and outputting evaluation data;

inputting the evaluation data to a circuit under test, performing a predetermined process based on the evaluation data, and outputting a result of the process as output data;

controlling a second selector based on a second selector control signal to output the other of the first clock signal and the second clock signal as a second operation clock signal; and

inputting the second operation clock signal to a second flip-flop and inputting the output data, operating the second flip-flop in synchronization with an edge of the inputted second clock signal, and outputting the output data inputted from the circuit under test.

14. The control method of the semiconductor integrated circuit according to claim 13, further comprising inputting the phase control signal, the first selector control signal, and the second selector control signal from outside of the semiconductor integrated circuit.

15. The control method of the semiconductor integrated circuit according to claim 14, wherein in a normal operation, the phase control signal, the first selector control signal, and the second selector control signal such that the first clock signal and the second clock signal are synchronized are inputted.

16. The control method of the semiconductor integrated circuit according to claim 15, wherein in an operation test, the phase control signal, the first selector control signal, and the second selector control signal such that a phase difference is formed between the first clock signal and the second clock signal are inputted.

17. A semiconductor integrated circuit, comprising:

a phase control circuit to which a first clock signal is inputted, and which shifts a phase of the first clock signal based on a phase control signal and outputs the resultant signal as a second clock signal;

a first selector to which the first clock signal and the second clock signal are inputted, and which outputs one of the first clock signal and the second clock signal as a first operation clock signal based on a first selector control signal;

an evaluation data generating circuit which generates evaluation data and outputs the evaluation data;

a first flip-flop to which the first operation clock signal and the evaluation data are inputted, and which operates in synchronization with an edge of the first operation clock signal and outputs the evaluation data;

a circuit under test to which the evaluation data is inputted, and which performs a predetermined process based on the evaluation data and outputs a result of the process as output data;

a second selector to which the first clock signal and the second clock signal are inputted, and which outputs the other of the first clock signal and the second clock signal as a second operation clock signal based on a second selector control signal;

a second flip-flop to which the second operation clock signal

is inputted and the output data is inputted, and which operates in synchronization with an edge of the second operation clock signal and outputs the output data inputted from the circuit under test;

an expected value comparison circuit to which the output data is inputted from the second flip-flop, and which compares an expected value expected from the evaluation data and the output data; and

a sequence circuit which controls the phase control circuit, the first selector, the second selector, the evaluation data generating circuit, and the expected value comparison circuit and, wherein the sequence circuit sequentially shifts a phase of the second clock signal so that a phase difference between the first clock signal and the second clock signal increases until the output data and the expected value become non-coincident when the output data and the expected value coincide in the expected value comparison circuit.

18. The semiconductor integrated circuit according to claim 17, wherein the phase control signal, the first selector control signal, and the second selector control signal are generated by the sequence circuit.

19. A control method of a semiconductor integrated circuit, comprising:

controlling a phase control circuit based on a phase control signal to shift a phase of a first clock signal and outputting the resultant signal as a second clock signal;

controlling a first selector based on a first selector control signal to output one of the first clock signal and the second clock signal as a first operation clock signal;

generating evaluation data in an evaluation data generating circuit and outputting the evaluation data from the evaluation data generating circuit;

inputting the first operation clock signal and the evaluation data to a first flip-flop, operating the first flip-flop

in synchronization with an edge of the first operation clock signal, and outputting the evaluation data;

inputting the evaluation data to a circuit under test, performing a predetermined process based on the evaluation data, and outputting a result of the process as output data;

controlling a second selector based on a second selector control signal to output the other of the first clock signal and the second clock signal as a second operation clock signal;

inputting the second operation clock signal and the output data to a second flip-flop, operating the second flip-flop in synchronization with an edge of the second clock signal, and outputting the output data inputted from the circuit under test;

inputting the output data from the second flip-flop to an expected value comparison circuit and comparing an expected value expected from the evaluation data and the output data; and

controlling the phase control circuit, the first selector, the second selector, the evaluation data generating circuit, and the expected value comparison circuit, and sequentially shifting a phase of the second clock signal so that a phase difference between the first clock signal and the second clock signal increases until the output data and the expected value become non-coincident when the output data and the expected value coincide in the expected value comparison circuit.

20. The control method of the semiconductor integrated circuit according to claim 19, further comprising generating the phase control signal, the first selector control signal, and the second selector control signal.